Enabling Compact Multi-Pixel Heterodyne Terahertz Receivers Using On-Chip Power-Combined Multiplied Sources

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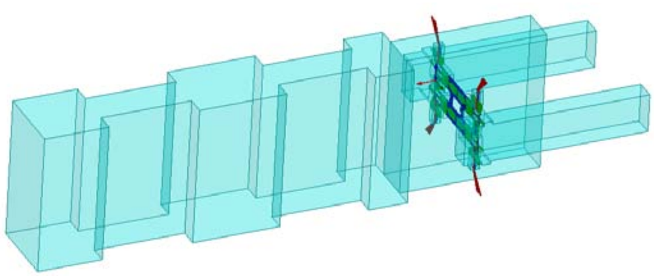
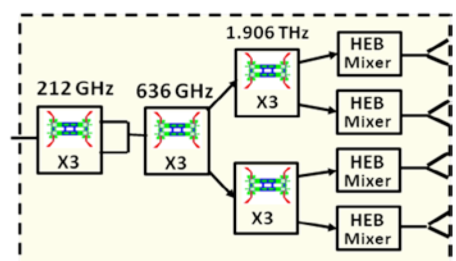
Abstract- The submillimeter-wave range is rich in emission and absorption lines of important molecular species, whose detection and mapping are important to understand the atmospheric circulation of planets, stars and galaxy formation, and pollution and its effects on our atmosphere. Instruments using high resolution heterodyne spectrometers are best suited to study these effects. The current generation heterodyne instruments for terahertz space missions primarily use single-pixel receivers driven by all-solid-state Schottky diode frequency multiplier based local oscillators. The next generation instruments should focus on multi-pixel configurations that allow doing more science during very limited time available for effective Terahertz observations [1]. However, current available sources have low overall efficiency and output power and are not suitable for multi-pixel operation.

With more than 30 µW already available at 1.9 THz from a single-pixel multiplied source developed at JPL, one of the immediate goals would be to develop a compact 4-pixel source module easily extendable to a higher number of pixels. Such a chain would have an immediate application to airborne or space observatories for a more efficient mapping of the C+ ond OI lines. For this task, the efficiency of the overall multiplier chain needs to be increased. High-power multipliers based on traditional device topologies require a very high number of chips to accommodate multiple diodes as well as multiple power-combining/dividing waveguide structures, which makes the integration not very efficient due to undesired waveguide losses and leads to a notable increase of the design effort and the receiver size, cost and volume

In this work we present the progress towards the development of a 1.9-2.1 THz multi-pixel source using the on-chip power combining concept introduced in [2]. This topology employs the 3D capabilities of Silicon micro-machining instead of classical metal block milled housing. Input and output waveguides are placed perpendicular to the waveguide where the diodes are located and four E-probes located in-phase at the input waveguide drive four multiplying structures integrated on a single chip (see Fig. 1a). Losses due to asymmetries are minimized since power-combining is performed 'on-chip'. Alignment and symmetry are no longer determined by the tolerances involved in the metal block machining and manual assembly of multiple chips, but by the superior precision of MMIC lithography. In addition, no Y-junctions or hybrid couplers are necessary to combine the signal as was required for multichip multipliers, considerably reducing the waveguide losses and enhancing generated power. Moreover, the 'on-chip' power-combining topology provides to independent outputs with tunable output power using the dc bias lines, enabling direct multi-pixel operation without any further circuitry. Using this topology, a very compact 4-pixel 1.9-2.1 THz multiplied source can be developed featuring only 4 multiplier chips and producing at least 10 uW of output power per pixel (see Fig. 1b).



(a)



(b)

Fig. 1. MIDAS high-power dual-chip single-waveguide 190 GHz doubler design (a) and expected performance (b)

The chips for the last two stages have been already fabricated in the JPL Micro Devices Laboratory and housing blocks for testing the individual design will be fabricated soon.

[1] V. Belitsky, V. Desmaris, D. Dochev, D. Meledin A. Pavolotsky, "Towards Multi-Pixel Heterodyne Terahertz Receivers," *Proc. of the 22nd International Symposium on Space Terahertz Technology*, Apr. 2011.

[2] J. V. Siles, B. Thomas, G. Chattopadhyay, A. Maestrini, C. Lee, E. Schlecht, C. Jung and I. Mehdi, "Design of a high-power 1.6 THz Schottky tripler using 'on-chip- power combining and Silicon micromachining," *Proc. of the 22th International Symposium on Space Terahertz Technology*, Apr. 2011.

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